Docket No.: M4065.0210/P210
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Sam Yang et al.

Application No.: 09/588,008 Confirmation No.: 9015

Filed: June 6, 2000 Art Unit: 2814

For: A CAPACITOR FOR A SEMICONDUCTOR DEVICE Examiner: H. B. Trinh

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As permissible under § 41.41, this brief is filed in furtherance of the Appellants' Appeal Brief Filed June 25, 2007.

This brief contains items under the following headings as required by 37 C.F.R. § 41.41 and M.P.E.P. § 1208:

I. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 32 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 32-98

2. Claims withdrawn from consideration but not canceled: None.

3. Claims pending: 1-31 and 99

4. Claims allowed: --[1]

5. Claims rejected: 1-31 and 99[2]

C. Claims On Appeal

The claims on appeal are claims 1-31 and 99.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 7-16, 18-25, 29-31 and 99 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,338,996 ("Iizuka").

Claims 4, 5 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh").

Claims 6 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers").

Claims 26 and 27 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Iizuka, or in the alternative, under 35 U.S.C. § 103(a) as being obvious over Iizuka, in view of U.S. Patent No. 6,475,854 ("Narwankar").

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[1] The Papers from the PTO are inconsistent and therefore it is unclear if any of the claims are allowable. According to the most recently issued Advisory Action in this case, mailed March 21, 2007, part of Paper No. 20070317, claims 1-31 and 99 stand rejected. In the Notice of Panel Decision from Pre-Appeal Brief Review, mailed March 24, 2007, part of Paper No. 20070522, claims 1-3, 7-16, 18-25, 29-31, and 99 stand rejected. The Notice does not indicate the status of claims 4-6, 17, and 26-28. For the purposes of the Appeal and out of an abundance of caution, Applicants presume claims 1-31 and 99 stand rejected. However, Applicants are not suggesting that claims 4-6, 17, and 26-28 are not in condition of allowance.

[2] See Footnote #1.

Claim 28 stands rejected under 35 U.S.C. § 102(e) as being anticipated by or Iizuka, in the alternative, under 35 U.S.C. § 103(a) as being obvious over Iizuka, in view of U.S. Patent No. 6,387,802 ("Marsh").

III. ARGUMENT

A. Claims 1-3, 7-16, 18-25, 29-31 and 99 are not anticipated by U.S. Patent No. 6,338,996 ("Iizuka"). Further, the Office has failed to completely address and respond to Appellants' arguments as stated in the Appeal brief and early PTO submissions.

Iizuka does not disclose all of the limitations of claim 1. Specifically, Iizuka does *not* disclose an *annealed* dielectric layer "annealed with a first annealing process" *and* an annealed top electrode "annealed with a second annealing process".

The Office suggests in the Examiner's Answer that the first annealing process is disclosed by Iizuka at col. 1, lines, 30-35, col. 2, lines 13-15; col. 4, lines 55-60. The Office also suggests in the Examiner's Answer that the second annealing process is disclosed by Iizuka at col. 2, line 33; and col. 5, lines 20-25. (cited passages set out in Applicant's Appellate Brief)

The Office still has not yet adequately responded to Appellant's arguments that the Examiner has pieced together different sections of Iizuka's patent disclosure in an attempt to achieve the claimed invention. In the Examiner's Answer, the Office still fails to address, because it cannot, the lack of two distinct annealing steps in Iizuka. Hence, at best, Iizuka only discloses one anneal performed, at a temperature lower than conventionally done, after the capacitor is formed. (See Iizuka specification for further description of only one anneal step being performed in the Iizuka method, that step being performed after the capacitor structure is formed: "...the formation of the capacitor is followed by anneal..." (Iizuka, Abstract); "...the method being characterized in that the formation of the capacitor is followed by anneal..." (Iizuka, Col. 2, lines 30-32); "...the method being characterized in that the formation of the capacitor is followed by anneal..." (Iizuka, Col. 2, lines 41-43); "after forming the high dielectric thin film capacitor, anneal is performed..." (Iizuka, Col. 4, lines 28-30); "...after the high dielectric thin film capacitor is formed, anneal is

performed..." (Iizuka, Col. 4, lines 57-59); and "as has been described above, according to the present invention, after formation of the capacitor, anneal is performed..." (Iizuka, Col. 5, lines 49-52))

The Office's inability to address the lack of two distinct annealing steps in Iizuka is due to Iizuka failing to disclose two distinct annealing steps. The Office in its Answer identifies a section in Iizuka's background discussion which discuss problems in the prior art when annealing at higher temperatures and thus suggests annealing at lower temperatures might be preferred. But, the Office still cannot identify the two annealing processes as claimed.

Additionally, it is also noted that during an Office interview held on February 21, 2007 in related case 10/002,176, the Office could not expressly identify the two annealing processes as claimed. Subsequent responses from the Office have not further identified a capacitor formed with two annealing processes in Iizuka.

Since the Office cannot identify in Iizuka "an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . ." and a "top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," Iizuka cannot anticipate claim 1. In the Examiner's Answer, the Office suggests that the "anneal" limitations of claim 1 are product-by-process limitations which are accorded little or no weight. However, claim 1 recites annealed structures in which the annealed structures have been annealed by two distinct anneal processes; accordingly, the anneal limitations are not product by process limitations.

Since Iizuka does not disclose all of the limitations of claim 1, claim 1 and claims 2-3, 7-16, 18-25 and 29-31 depending therefrom are not anticipated by Iizuka.

Claim 99 recites similar limitations to claim 1, including, *inter alia*, "an annealed dielectric layer . . . that has been annealed with a first oxidizing gas anneal process; and an upper electrode . . . which is an oxidized gas annealed layer formed over said annealed dielectric layer that

has been annealed with a second oxidizing gas anneal process." For at least the same reasons as discussed with respect to claim 1, claim 99 is not anticipated by Iizuka.

A reversal of the rejections of claims 1-3, 7-16, 18-25, 29-31, and 99 as being anticipated by Iizuka is respectfully requested.

B. Claims 4, 5 and 17 are not unpatentable under 35 U.S.C. § 103(a) over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh"). Further, the Office in its Examiner's Answer has failed to completely address and respond to Appellants' arguments as stated in the Appeal brief and early PTO submissions.

Claim 4 recites, *inter alia*, "...wherein said bottom conducting layer is formed of a metal alloy."

Claim 5 recites, *inter alia*, "...wherein said bottom conducting layer is formed of a conducting metal oxide."

Claim 17 recites, *inter alia*, "...wherein said top conducting layer is formed of a conducting metal oxide."

Claims 4, 5 and 17 depend from claim 1 and are similarly allowable over Iizuka for at least the reasons provided above with regard to claim 1.

As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Emesh discloses forming a capacitor within a via hole. Emesh does not cure the noted deficiencies of Iizuka as Emesh does not teach or suggest the subject matter of claim 1.

The Office in its Answer, by contrast, continues to asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the bottom electrode of Iizuka with the metal alloy or conductive metal oxide material, as taught by Emesh, so as to provide an alternative material to make the bottom electrode." (Answer, p. 6) And yet, the Office does not, and has not addressed the issue that Iizuka actually *teaches away* from this combination.

As previously argued, Iizuka teaches that *both* electrodes in the capacitor should consist of a *noble metal*; hence, Iizuka teaches away from substituting Emesh's metal alloy, or a conducting metal oxide for either the upper or lower electrodes, and thus there is no motivation to combine the teachings of Iizuka and Emesh. The Examiner's Answer, however, fails to address this issue of Iizuka teaching away from Emesh and only provides a conclusionary response that states simply: Iizuka + Emesh = the claimed invention. Therefore, the Office responds the only way it can when it fails to show objective evidence or support, it summarily indicates that "it would have been obvious..." without any further support. As Iizuka teaches away from any motivation to combine, the Office has failed to meet its burden on this issue.

Since the cited references do not teach or suggest all the limitations of claim 1, claims 4, 5 and 17 depending therefrom are patentable over the reference. Furthermore, the Office has not identified any motivation in either Emesh or Iizuka to combine their divergent teachings in order to achieve the claimed invention or ignore the express teachings in Iizuka of using noble metal electrode for both the top and bottom electrodes of a capacitor. This is another reason why claims 4, 5 and 17 are patentable.

Accordingly, a reversal of the 35 U.S.C. § 103 rejection of claims 4, 5, and 17 is respectfully requested.

C. Claims 6 and 14 are not unpatentable under 35 U.S.C. § 103(a) over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers"). Further, the Office in its Examiner's Answer has failed to

completely address and respond to Appellants' arguments as stated in the Appeal brief and early PTO submissions.

Claim 6 recites, *inter alia*, "...wherein said bottom conducting layer is formed of a metal nitride."

Claim 14 recites, *inter alia*, "....wherein said top conducting layer is formed of a material selected from the noble metal group."

Claims 6 and 14 depend from claim 1 and are similarly allowable over Iizuka for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Alers does not cure the noted deficiencies of Iizuka as Alers does not disclose a capacitor formed by two separate anneal processes.

The Office in its Answer asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the invention of Iizuka with the bottom electrode made of metal nitride, as taught by Alers, so as to provide an alternative material for the bottom electrode."(Answer, p. 7) However, as noted above, Iizuka *teaches away* from such a combination, requiring use of noble metals for upper and lower electrodes, which is not addressed in the Office's Answer. As such, Alers cannot be combined with Iizuka since Iizuka teaches away from any material other than noble metals for a bottom electrode. Again, the Office has failed to adequately address this issue and therefore has failed to satisfy its burden of proof. Accordingly, the references do not teach or suggest all the limitations of claim 1 and claims 6 and 14 depending therefrom.

Accordingly, a reversal of the 35 U.S.C. § 103 rejection of claims 6 and 14 is respectfully requested.

D. Claims 26 and 27 are not anticipated under 35 U.S.C. § 102(e) by Iizuka, or in the alternative, unpatentable under 35 U.S.C. § 103(a) as being obvious over Iizuka, in view of U.S. Patent No. 6,475,854 ("Narwankar"). Further, the Office has failed to completely address and respond to Appellants' arguments as stated in the Appeal brief and early PTO submissions.

Claim 26 recites, *inter alia*, "...wherein said annealed top conducting layer is a plasma enhanced annealed top conducting layer."

Claim 27 recites, *inter alia*, "...wherein said annealed top conducting layer is a remote plasma enhanced annealed top conducting layer."

Claims 26 and 27 depend indirectly from claim 1 and are similarly allowable over Iizuka for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Accordingly, to the extent that this rejection is one of anticipation by Iizuka, a reversal is respectfully requested.

Narwankar discloses a plasma enhanced annealed layer, but does not disclose "an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1. This is not adequately addressed by the

Office in its Answer Brief. Since neither Iizuka nor Narwankar, teach or suggest all of the limitations of claim 1, claims 26 and 27 depending therefrom are patentable over the cited combination. Further, as noted above and previously noted, claim 1 is not a product by process. Accordingly, to the extent that this rejection is under § 103 based on the teachings of Iizuka in view of Narwankar, a reversal is respectfully requested.

E. Claim 28 is not anticipated under 35 U.S.C. § 102(e) by Iizuka or, in the alternative, unpatentable under 35 U.S.C. § 103(a) as being obvious over Iizuka, in view of U.S. Patent No. 6,387,802 ("Marsh"). Further, the Office in its Examiner's Answer has failed to completely address and respond to Appellants' arguments as stated in the Appeal brief and early PTO submissions.

Claim 28 recites, *inter alia*, "...wherein said annealed top conducting layer is an ultraviolet light enhanced annealed top conducting layer."

Claim 28 depends from claim 1 and is similarly allowable over Iizuka for at least the reasons provided above with regard to claim 1, and on its own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Iizuka also fails to disclose an ultraviolet enhanced annealed top electrode and thus can not anticipate claim 28 for this additional reason. Accordingly, to the extent that the rejection of claim 28 is based on anticipation by Iizuka, a reversal of the rejection is respectfully requested.

Marsh discloses a "method of depositing a platinum based metal film by CVD deposition includes bubbling a non-reactive gas through an organic platinum based metal precursor to facilitate transport of precursor vapor to the chamber. The platinum based film is deposited onto a non-silicon bearing substrate in a CVD deposition chamber in the presence of ultraviolet light at a

predetermined temperature and under a predetermined pressure. The film is then annealed in an oxygen atmosphere at a sufficiently low temperature to avoid oxidation of substrate. The resulting film is free of silicide and consistently smooth and has good step coverage." (Marsh, Abstract)

Marsh also fails to cure the inadequacies of Iizuka and does not teach or suggest a capacitor comprising a "bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added). Nor has there been provided in the references, the motivation or ability to combine the references to achieve the claimed invention. Accordingly, to the extent that the rejection of claim 28 is under 35 U.S.C. § 103 based on the teachings of Iizuka in view of Marsh, a reversal of the rejection is respectfully requested.

For the reasons advanced, claims 1-31 and 99 are not anticipated by or rendered obvious over the prior art cited in the various rejections of the claims. Accordingly, a reversal of all rejections is respectfully requested.

IV. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

Dated: December 3, 2007

Respectfully submitted,

By #41,198

Thomas J. D'Amico
Registration No.: 28,371
Michael A. Weinstein
Registration No.: 53,754
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant/Appellant

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/588,008

1. A capacitor for a semiconductor device, said capacitor comprising:

a bottom conducting layer, wherein said bottom conducting layer is a bottom electrode;

an annealed dielectric layer formed over said bottom conducting layer, wherein said annealed dielectric layer is annealed with a first annealing process; and

a top electrode consisting of a single oxidized gas annealed top conducting layer formed over said annealed dielectric layer, wherein said annealed top conducting layer is annealed with a second annealing process.

2. The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

3. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal.

4. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal alloy.

5. The capacitor of claim 1, wherein said bottom conducting layer is formed of a conducting metal oxide.

6. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal nitride.

7. The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2). Chromium Oxide

(CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WNx, WN, or W2N).

8. The capacitor of claim 7, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WNx, WN, or W_2N).

9. The capacitor of claim 1, wherein said bottom conducting layer is placed on top of an oxygen barrier.

10. The capacitor of claim 1, wherein said dielectric layer is a dielectric metal oxide layer.

11. The capacitor of claim 1, wherein said dielectric layer has a dielectric constant between 7 and 300.

12. The capacitor of claim 1, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (BST), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3) and Zirconium Silicate.

13. The capacitor of claim 12, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (SBT), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2).

14. The capacitor of claim 13, wherein said dielectric layer is Tantalum Oxide and is amorphous or crystalline.

15. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the noble metal group.

16. The capacitor of claim 1, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

17. The capacitor of claim 1, wherein said top conducting layer is formed of a conducting metal oxide.

18. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from die group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2).

19. The capacitor of claim 18, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

20. The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

21. The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and, said dielectric layer is a layer of Barium Strontium Titanate (BST).

22. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the group consisting of Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and, said bottom conducting layer is a layer of Tungsten Nitride (WNx, WN, or W_2N) layer and, said dielectric layer is a layer of Aluminum Oxide (Al_2O_3).

23. The capacitor of claim 1, wherein said top conducting layer is annealed with an oxygen compound.

24. The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a material selected from the group consisting of: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

25. The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a gas mixture containing at least one element selected from the group consisting: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

26. The capacitor of claim 23, wherein said annealed top conducting layer is a plasma enhanced annealed top conducting layer.

27. The capacitor of claim 23, wherein said annealed top conducting layer is a remote plasma enhanced annealed top conducting layer.

28. The capacitor of claim 23, wherein said annealed top conducting layer is an ultraviolet light enhanced annealed top conducting layer.

29. The capacitor of claim 1, wherein said capacitor is a stacked capacitor.

30. The capacitor of claim 1, wherein further comprising an access transistor connected to said capacitor.

31. The capacitor of claim 1, wherein said capacitor forms part of a dynamic random access memory cell.

99. A capacitor for a semiconductor device, said capacitor comprising:

a bottom electrode;

an annealed dielectric layer formed over said bottom electrode that has been annealed with a first oxidizing gas anneal process; and

an upper electrode comprising a top conducting layer which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process.